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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1		("6326809").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/02/06 22:59
L2	1166	architectural adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:05
L3	70	L2 same (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:18
L4	369862	detect\$3 near3 (error\$5 or fault\$3 or problem or malfunction or fail\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:07
L5	19	3 and L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:07
L6	3698	(lead\$3 or trail\$3) adj thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:08
L7	50	synchroniz\$4 same 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:09
L8	2	5 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:16

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L9	114	2 and (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:38
L10		9 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:19
L11	5	10 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:19
L12		11 and synchroniz\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/02/06 23:36
L13	214	((lead\$3 or primary) adj thread) same ((trail\$3 or secondary or fowing) adj thread)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:38
L14	1	13 same (checkpoint\$3 or check-point\$3) same validat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR ·	ON	2007/02/06 23:39
L15	2	13 and (checkpoint\$3 or check-point\$3) and validat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:39
L16 <sup>-</sup>	556	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2007/02/06 23:43

L17	965	(714/2).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/02/06 23:42
L18	985	(714/15).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:42
L19	1881	(714/38).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:42
L20	232	(714/16).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2007/02/06 23:42
L21	1	(L16 or L17 or L18 or L19 or L20) and 7 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:44
L22	570	(712/218).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:43
L23	0	22 and 7 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:44
S1	509	(714/13).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 16:36

S2	922	(714/2).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2006/07/26 14:48
S3	935	(714/15).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 14:49
S4	1713	(714/38).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:41
. S5	220	(714/16).ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 15:01
S6	69	(reinhardt-steven\$ or mukherjee-shubhendu\$ or emer-joel\$).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 15:10
S7	4882	hardware same (error\$5 or fault\$3 or problem or malfunction or fail\$4) same recover\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON ·	2006/07/26 17:16
S8	8445	multi-thread\$4 or (multi adj thread\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR ·	ON	2006/07/26 15:20
59	6	S7 same S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR <sub>.</sub>	ON	2006/07/26 16:13

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S10	0	S9 same (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/02/06 23:05
S11	49	S7 and S8 and (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:11
S12	3632	(lead\$3 or trail\$3) adj thread	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 16:13
S13	3	S11 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 16:13
S14	8	(("6058491") or ("6317821") or ("6519730") or ("20010034854")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR .	OFF	2006/07/26 17:03
S15	1065	architectural adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:03
S16	45	non-deterministic adj event	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:11
S17	4	S15 and S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2006/07/26 17:11

S18	4	S17 and (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:33
S19	46856	(recover\$3 or restor\$3 or recaptur\$3 or re-execut\$3) near3 state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:14
S20	13	S19 same S16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:14
S21	13	S20 and (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR .	ON	2006/07/26 17:34
S22	351935	detect\$3 near3 (error\$5 or fault\$3 or problem or malfunction or fail\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:17
S23	13	S21 and S22	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2006/07/26 17:32
S24	16	(lead\$3 or trail\$3) adj thread adj execut\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	ÖR	ON	2007/02/06 23:08
S25	127	validat\$3 near3 (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:33

S26		S24 same S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:34
S27		S24 and S25	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:34
S28	3	S24 and (checkpoint\$3 or check-point\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON .	2006/07/26 17:35
S29	13	S24 and synchroniz\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/26 17:35

\*Results (page 1): hardware and recovery and multi-thread and leading thread and trailing thread and checkp... Page 1 of 7 Subscribe (Full Service) Register (Limited Service, Free) Search: • The ACM Digital Library • C The Guide hardware and recovery and multi-thread and leading thread ar Feedback Report a problem Satisfaction survey Found Terms used 13,624 of hardware and recovery and multi thread and leading thread and trailing thread and checkpoint 196,064 Try an Advanced Search Sort results Save results to a Binder relevance Try this search in The ACM Guide by Search Tips Display expanded form results Open results in a new window Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 Best-200 shown Relevance scale SMTp: An Architecture for Next-generation Scalable Multi-threading Mainak Chaudhuri, Mark Heinrich March 2004 ACM SIGARCH Computer Architecture News, Proceedings of the 31st annual international symposium on Computer architecture ISCA '04, Volume 32 Issue 2 Publisher: IEEE Computer Society, ACM Press Full text available: pdf(247.58 KB) Additional Information: full citation, abstract We introduce the SMTp architecture-an SMT processoraugmented with a coherence protocol thread context, that together with a standard integrated memory controllercan enable the design of (among other possibilities) scalablecache-coherent hardware distributed shared memory(DSM) machines from commodity nodes. We describe theminor changes needed to a conventional out-of-order multi-threadedcore to realize SMTp, discussing issues related toboth deadlock avoidance and performance. We then compareSMTp p ... State saving for interactive optimistic simulation Steve Franks, Fabian Gomes, Brian Unger, John Cleary June 1997 ACM SIGSIM Simulation Digest, Proceedings of the eleventh workshop on Parallel and distributed simulation PADS '97, Volume 27 Issue 1 Publisher: IEEE Computer Society, ACM Press Full text available: Additional Information: full citation, abstract, references, citings, index Publisher Site Time Warp's optimistic scheduling requires the maintenance of simulation state history to support rollback in the event of causality violations. State history, and the ability to rollback the simulation, can provide unique functionality for human-in-the-loop simulation environments. This paper investigates the use of Time Warp to output valid simulation

state in a near real-time manner, re-execute portions of the simulation, and interactively probe simulation values to ascertain underlying cause ...

3 Dynamically allocating processor resources between nearby and distant ILP

Rajeev Balasubramonian, Sandhya Dwarkadas, David H. Albonesi

May 2001 ACM SIGARCH Computer Architecture News, Proceedings of the 28th annual international symposium on Computer architecture ISCA '01, Volume

29 Issue 2

Publisher: ACM Press



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A survey of rollback-recovery protocols in message-passing systems



E. N. (Mootaz) Elnozahy, Lorenzo Alvisi, Yi-Min Wang, David B. Johnson September 2002 ACM Computing Surveys (CSUR), Volume 34 Issue 3

Publisher: ACM Press

Full text available: pdf(549.68 KB)

Additional Information: full citation, abstract, references, citings, index terms, review

This survey covers rollback-recovery techniques that do not require special language constructs. In the first part of the survey we classify rollback-recovery protocols into checkpoint-based and log-based. Checkpoint-based protocols rely solely on checkpointing for system state restoration. Checkpointing can be coordinated, uncoordinated, or communication-induced. Log-based protocols combine checkpointing with logging of nondeterministic events, encoded in tuples call ...

**Keywords**: message logging, rollback-recovery

82 Threads: Balancing register pressure and context-switching delays in ASTI systems



Siddhartha Shivshankar, Sunil Vangara, Alexander G. Dean

September 2005 Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems CASES '05

Publisher: ACM Press

Full text available: pdf(261.60 KB)

Additional Information: full citation, abstract, references, citings, index

This paper makes two contributions to Asynchronous Software Thread Integration (ASTI). First, it presents methods to calculate worst-case secondary thread performance statically. This will enable real-time performance quarantees for the system in future work. Second, it improves the run-time performance of integrated threads by partitioning the register file, allowing faster coroutine calls. Determining the ideal partitioning of the register file is non-trivial if the registers are heterogeneous ...

**Keywords**: asynchronous software thread integration, fine-grain concurrency, hardware to software migration, software-implemented-communication protocols

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